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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/583,868	06/21/2006	Tetsuya Hirano	292813US2PCT	8990
22850 7590 04/29/2009 OBLON, SPIVAK, MCCLELLAND MAIER & NEUSTADT, P.C. 1940 DUKE STREET ALEXANDRIA, VA 22314			EXAMINER GIARDINO JR, MARK A	
			ART UNIT	PAPER NUMBER
			2185	
			NOTIFICATION DATE	DELIVERY MODE
			04/29/2009	ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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**DETAILED ACTION**

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2/17/2009 has been entered.

The Examiner acknowledges the applicant's submission of the amendment dated 2/17/2009.

The instant application having Application No. 10/583,868 has a total of 4 claims pending in the application, there are 4 independent claims and 0 dependent claims, all of which are ready for examination by the examiner.

**OBJECTIONS TO THE SPECIFICATION**

Specific references to the claims in the specification must be corrected such that what is said in the specification remains consistent with the amended claims. Such references include:

Page 6, Line 12 ("As defined in Claim 2"), where a reference is subsequently made in the specification to the control means allowing the CPU "to access the external memory by utilizing a free bus cycle", which is no longer recited in Claim 2. Appropriate correction is required to pages 7-8 such that the description in the specification of Claim 2 coincides with claim 2 as amended 2/17/2009.

Page 8, Line 24-25 (“the structure defined in Claim 3”), where a reference is subsequently made in the specification to a read/write control means controls, which controls the command of which DSP is allowed, which is no longer recited in Claim 3. Appropriate correction is required to pages 8-10 such that the description in the specification of Claim 3 coincides with claim 3 as amended 2/17/2009.

Page 10, Line 15 (“As defined in Claim 5”), where a reference is subsequently made in the specification to a read/write control means controls, which controls the command of which DSP is allowed, which is no longer recited in Claim 5. Appropriate correction is required to pages 10-11 such that the description in the specification of Claim 3 coincides with claim 3 as amended 2/17/2009.

The paragraph on Page 11 Line 26 to Page 12 Line 3 makes reference to now cancelled claims 4 and 6, and must be corrected.

Page 12, Line 15 makes reference to now cancelled claims 4 and 6 and must be corrected.

Page 12, Line 24 makes reference to now cancelled claim 6 and must be corrected.

## **ARGUMENTS CONCERNING PRIOR ART REJECTIONS**

### **Rejections - USC 102/103**

Applicant's argument with respect to claims 1-3 and 5 has been considered and has distinguished the applicant's invention from the prior art of record.

Thusly, the rejections of claims 1-3 and 5 have been withdrawn.

### **STATEMENTS OF REASONS FOR ALLOWANCE**

The following is an examiner's statement of reasons for allowance:

The primary reason for allowance of **Claim 1** rest in the combination with the inclusion of the following limitation of:

“when the DSP accesses the external memory using a maximum number of the bus cycles in a unit of data access wherein the DSP actually accesses the external memory, access from the CPU to the external memory is placed in a wait state until a subsequent unit of data access commences, and

when the DSP does not access the external memory using the maximum number of the bus cycles in said unit of data access wherein the DSP actually accesses the external memory, access from the CPU to the external memory is constantly allowed during said unit of access”.

The primary reason for allowance of **Claim 2** rest in the combination with the inclusion of the following limitation of:

“when the DSP accesses the external memory using a maximum number of the bus cycles in a unit of data access wherein the DSP actually accesses the external memory, access from the CPU to the external memory is placed in a wait state until a subsequent unit of data access commences, and

when the DSP does not access the external memory using the maximum number

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of the bus cycles in said unit of data access wherein the DSP actually accesses the external memory, access from the CPU to the external memory is constantly allowed during said unit of access".

The primary reason for allowance of **Claim 3** rest in the combination with the inclusion of the following limitation of:

"a read/write control unit configured so that when each of the DSPs issues a read command or a write command at a same time, none of the commands from the DSPs are performed".

The primary reason for allowance of **Claim 5** rest in the combination with the inclusion of the following limitation of:

"a read/write control unit configured so that when each of the DSPs issues a read command or a write command at a same time, none of the commands from the DSPs are performed".

These limitations above are taught by the specification at least on Page 24, Lines 22-27, and Page 42, Lines 24-27 of Applicant's specification and are argued on pages 9-10 of the applicant's remarks/arguments dated 17 February 2009. The subject matter recited in claims 1-3 and 5 are not taught or suggested by the prior art of record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

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accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

## **CLOSING COMMENTS**

### **Conclusion**

## **STATUS OF CLAIMS IN THE APPLICATION**

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. ' 707.07(i)**:

### **SUBJECT MATTER CONSIDERED ALLOWABLE**

Claims 1-3 and 5 are considered patentably distinguishable over the prior art of record.

As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

## **DIRECTION OF FUTURE CORRESPONDENCES**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to M. Anthony Giardino whose telephone number is (571) 270-3565 and can normally be reached on Monday - Thursday 7:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Sanjiv Shah can be reached on (571) 272 - 4098. The fax phone

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number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

M.A. Giardino

/Stephen Elmore/  
Primary Examiner, Art Unit 2185

/M. A. G./

Examiner, Art Unit 2185

4/23/2009